3-0004-9

digital INTEROFFICE MEMORANDUM

DATE: 5 March 1969

SUBJECT: PDP-11 Electrical Design Review (Second Session)

TO: PDP-11 Design Review Committee FROM: Jerry Butler
CC: Engineering Committee
Roger Cady
Nick Mazzarese

The second session of the Design Review was held on Monday, 24 February 1969. Present were: G. Saviers, I. Morris, R. Best, G. Fligg, R. Cady, A. Kotok, R. Pyle, W. Moroney (for D. Dubary).

Comments On Last Meeting Minutes

Roger Cady said that the market for the PDP-11 should include the single user as well as O.E.M.

New Topics

Discussion continued on the addressing scheme. Roger outlines some changes to the addressing format. Copies of these changes were passed out at the meeting.

The committee commented that the new scheme takes away the ability to address the major registers in the address field easily for register to register operations (using a single byte address).

Roger recommended that a set of register to register instructions is being considered for addition to the machine.

It was commented that perhaps the auto increment capability would be more useful incrementing memory instead of the hardware registers.

Load byte was discussed again, and most agreed that load byte should copy the sign into the upper byte (contrary to our previous comment), as long as all byte instructions did something consistent with the sign. Also, since ASCII characters are really 7-bit characters, the sign bit shouldn't give much trouble when handling characters.

Mnemonics for inclusive ~~or~~ and jump to subroutine instructions were discussed. Inclusive should include "inclusive" in the mnemonics (IOR). The jump to subroutine instructions should have a mnemonic different than other DEC machines as it behaves differently(i.e. don't use JSR, JMS, etc.).

The break point jump facility should go to a fixed location in page Ø but not location zero.

A comment was made suggesting doing away with increment and decrement AC instructions and adding more sophisticated rotates or leave open holes in the op code for future expansion.

Alan Kotok suggested considering a "multiply step" instruction (like the PDP-1), to the machine to improve subroutine multiples.

It was pointed out that register N and bit N of the condition codes may have a name conflict when trying to document the machine.

Topics for the next meeting (April 5, 1:00 PM, N. Mazzarese's Conference Room) include:

1. More on architecture and instruction set
2. I/O philosophy and sequences

Please notify me if any errors or omissions have been made in these minutes.